IN THE CLAIMS

1. (Withdrawn) A semiconductor device comprising:

an insulating film formed on a semiconductor substrate having a bitline contact and a groove-shaped bitline pattern;

a bitline that is surrounded by the insulating film and formed on the bitline contact and in a portion of the bitline pattern; and

a bitline capping layer protruding from the insulating film and formed on the bitline within the bitline pattern and the insulating film, wherein a protruded portion of the bitline capping layer is wider than a width of the bitline.

2. (Withdrawn) The semiconductor device of claim 1, the bitline capping layer comprising:

a pillar-type first capping material formed on the bitline within the bitline pattern that protrudes from the insulating film; and

a sidewall spacer type second capping material formed on a protruded portion of the first capping material on the insulating film.

3. (Withdrawn) The semiconductor device of claim 2, wherein the protruded portion of the first capping material is approximately half the thickness of the first capping material.

4. (Withdrawn) The semiconductor device of claim 1, wherein the bitline capping layer has a stud type structure and comprises a material having a wet and a dry etching selectivity with respect to the insulating film.

5. (Withdrawn) The semiconductor device of claim 4, wherein the material comprises a film from a silicon nitride film series, and the insulating film comprises a film from an oxide film series.

6. (Currently amended) A method of fabricating a semiconductor device comprising:

forming an insulating film on a semiconductor substrate;

~~forming a bitline contact and a groove-shaped bitline pattern by~~ etching the insulating film to form a bitline contact hole and a groove-shaped bitline pattern;

forming a bitline ~~on~~ that fills the bitline contact hole and that fills a portion of the bitline pattern; and

forming a bitline capping layer on the bitline ~~within the bitline pattern and the insulating film that protrudes from the insulating film~~ that fills a remaining portion of the bitline pattern and that has a protruded portion that extends above a surface of the insulating film, wherein ~~a protruded~~ the protruded portion ~~of the bitline capping layer~~ is wider than ~~a width of~~ the bitline.

7. (Currently amended) The method of claim 6, wherein forming the bitline capping layer comprises:

depositing a first capping material on ~~an entire surface~~ a surface of the substrate;

etching the first capping material to fill within the bitline pattern on the bitline;

etching the insulating film to a predetermined thickness so that a portion of the first capping material protrudes above the insulating film;

depositing a second capping material on an entire surface of the substrate; and

etching the second capping material so that it remains only on a sidewall of the portion of the first capping material.

8. (Original) The method of claim 7, wherein etching the insulating film to the predetermined thickness comprises etching the insulating film to the predetermined thickness so that the portion of the first capping material is approximately half the thickness of the first capping material.

9. (Original) The method of claim 7, wherein depositing the first capping material and depositing the second capping material comprises depositing a material having a wet and a dry etching selectivity with respect to the insulating film.

10. (Currently amended) The method of claim 9, wherein depositing the first and second capping material comprises depositing a film from a silicon nitride film series, and forming the insulating film comprises forming a film from an oxide film series.

11. (Original) The method of claim 6, wherein forming the bitline capping layer comprises:

forming a pillar-type first capping material on the bitline within the bitline pattern that protrudes from the insulating film; and

forming a sidewall spacer type second capping material on a portion of the first capping material that protrudes from the insulating film, and

forming the pillar-type first capping material and forming the sidewall spacer type second capping material so that the bitline capping layer has a stud type structure.

12. (Original) The method of claim 6, wherein forming the bitline comprises:

depositing a conductive material on an entire surface of the substrate to fill the bitline pattern; and

over-etching the conductive material using at least one process chosen from the group consisting of a CMP process and a etch back process so that the conductive material fills up a portion of the bitline pattern to form the bitline.

13. (Currently amended) The method of claim 7, wherein forming the insulating ~~layer~~ film comprises:

forming an upper oxide film;

forming a lower oxide film; and

forming a silicon nitride film between the upper and the lower oxide films.

14. (Currently amended) The method of claim 13, wherein ~~forming the bitline capping layer~~ etching the insulating film comprises:

etching the upper oxide film using the silicon nitride film as an etching stop film.

15. (Original) The method of claim 13, wherein etching the second capping material comprises:

etching the lower oxide film so that it remains under the second capping material.

16. (Currently amended) The method of claim 6, wherein forming the bitline contact hole and the groove-shaped bitline pattern by etching the insulating film comprises using a dual damascene process, wherein the order in which the bitline pattern and the bitline contact hole are formed may be ~~reversed~~ alternated.

17. (Currently amended) A method of fabricating a semiconductor device comprising:

forming a first insulating film having a bitline contact pad and a storage node contact pad on a semiconductor substrate;

forming a second insulating film on ~~an entire surface~~ a surface of the substrate;

~~forming a groove-shaped bitline pattern and a bitline contact hole that exposes the bitline contact pad by~~ etching the second insulation film to form a groove-shaped bitline pattern and a bitline contact hole that exposes the bitline contact pad;

forming a bitline ~~in~~ that fills a portion of the bitline pattern and that is connected with the bitline contact pad through the bitline contact hole;

forming a bitline capping layer on the bitline ~~within~~ that fills a remaining portion of the bitline pattern and ~~the insulating film that protrudes from~~ that has a protruded portion that extends above a surface of the second insulating film, wherein ~~a protruded~~ the protruded portion is wider than ~~a width of~~ the bitline pattern;

forming a third insulating film on ~~an entire surface~~ a surface of the substrate; and

~~forming a storage node contact that exposes the storage node contact pad by~~ etching the second and the third insulating films to form a storage node contact hole that exposes the storage node contact pad.

18. (Currently amended) The method of claim 17, wherein forming the groove-shaped bitline pattern and the bitline contact hole comprises using a dual damascene process, wherein the order in which the bitline pattern and the bitline contact hole are formed may be ~~reversed,~~ alternated, and wherein the bitline contact pad is used as an etching stop film to form the bitline contact hole.

19. (Original) The method of claim 17, wherein forming the bitline capping layer comprises:

forming a pillar type first capping material on the bitline within the bitline pattern that protrudes from the second insulating film; and

forming a sidewall spacer type second capping material on a protruded portion of the first capping material and on the second insulating film,

wherein the protruded portion of the bitline capping layer has a stud type structure.

20. (Currently amended) The method of claim 19, wherein forming the storage node contact hole comprises:

etching the second and the third insulating films using the second capping material of the bitline capping layer as an etching stop film so that the storage node contact is self-align etched.